A Monolithic 6 GHz Quadrature Frequency Doubler With Adjustable Phase Offset

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***Abstract*—A 6 GHz frequency doubler with quadrature outputs generated from a differential single phase input is presented. The phase offset between the in-phase and quadrature outputs can be digitally controlled in linear steps for use in an automated calibration algorithm. The design nominally achieves standard deviations in quadrature phase error and amplitude balance of 0.4° and 0.1 dB, respectively. This is demonstrated with a single sideband (SSB) mixer that realizes an average uncalibrated sideband rejection of 48.2 dB which improves to 55.8 dB post-calibration under nominal conditions.**

***Index Terms*—Frequency conversion, mixers, phase noise, phase shifters, tranceivers, wireless LAN.**

I. Introduction

INCREASING traffic in the unlicensed ISM bands has given rise to the development of products dedicated to efficient spectral management and interference mitigation in WLAN systems [1]. One means of improving data throughput in a WLAN network is to use full duplex RF front-ends, requiring careful design to limit receive desensitization due to transmit noise and conversely transmit error vector magnitude (EVM) degradation due to receiver local oscillator (LO) leakage to the transmit path.

Frequency pulling is a concern in a full duplex system where receive and transmit voltage-controlled oscillators (VCOs) must operate simultaneously and be close in frequency [2]. This risk can be reduced by using a frequency doubler following one of the VCOs, thus allowing their center frequencies to be well separated. When this is done, the VCO resonator tank signals, the largest signals on the chip, have the strongest inband interferer limited to a low level second harmonic of the VCO operating at half frequency.

A frequency doubler following a VCO allows the synthesizer RF division ratio to be lower, and also allows the VCO to operate at half frequency. Both these factors reduce LO phase noise, offsetting the 6 dB noise penalty incurred by using a doubler.

When the receiver and transmitter operate simultaneously, the unwanted transmit sideband couples to the receive antenna causing receiver desensitization as shown in Fig. 1. In this scenario, the transmit channel is centered at f_{TX} while simultaneously the receiver detects a weak signal at f_{RX}. The added interference from the coupled sideband cannot generally be removed with a channelizing filter.

In a typical 802.11a application, if the transmit power is $+15$ dBm, transmit/receive isolation is 50 dB, minimum received level is -70 dBm, and a 20 dB SNR is required, then the required transmit sideband suppression is 55 dB. This translates into a required I/Q phase balance on the order of 0.2°. Even with judicious layout, such low phase error is difficult to reliably achieve unless provisions are made for calibration.

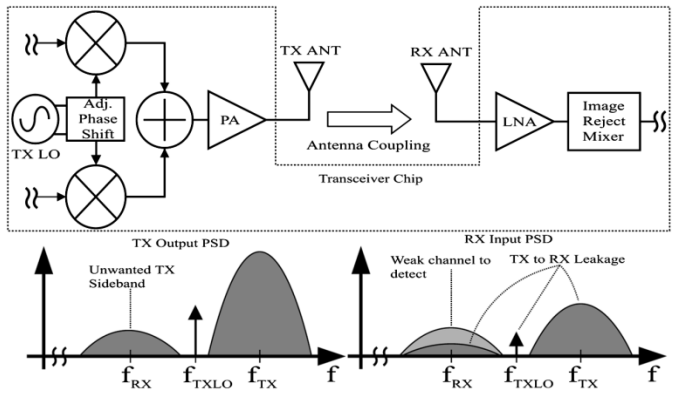

Fig. 1. Receiver desensitization due to transmit sideband leakage.

Regenerative frequency doublers [3], [4] have been proposed due to their great economy of power dissipation and die area. Since such doublers are essentially injection-locked oscillators, their lock range and spurious performance depend on the level of the injection input. When a frequency divider is used to obtain I and Q LO signals as in [4], an additional doubling is required, so care must be taken to ensure that the two oscillators do not interact undesirably.

A feedforward topology that does not use regenerative feedback was reported in [5]. This design has an inherent amplitude imbalance and DC offset that must be removed. The design exhibits low nominal phase errors but does not provide phase offset tuning.

In this paper, a frequency doubler architecture is presented that does not rely on injection locking or use tuned circuits. Sensitivity to input level is greatly reduced compared with existing doubler topologies, and five-bit phase quadrature tuning is provided to overcome normal process variations.

Section II discusses the background of existing frequency doublers and the architecture of the new doubler. Section III describes the simulated and measured performance of the new doubler.

II. Architecture

A. Frequency Doubler

If only a single phase LO is required, the frequency can be doubled by mixing the LO signal with itself with arbitrary phase

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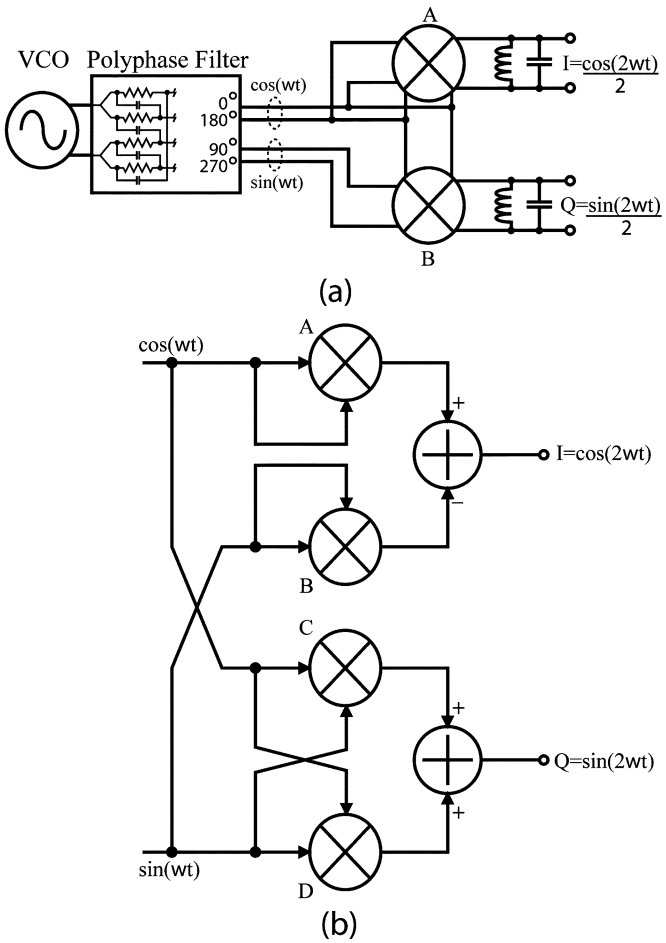

Fig. 2. (a) Simple quadrature frequency doubler. (b) Modified doubler with no DC offset and balanced polyphase filter load.

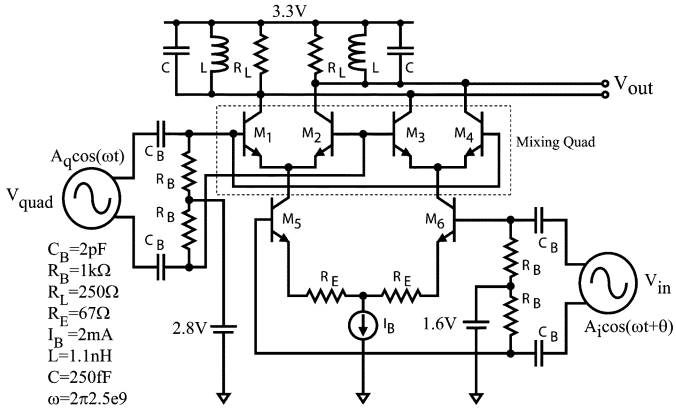

Fig. 3. Gilbert mixer.

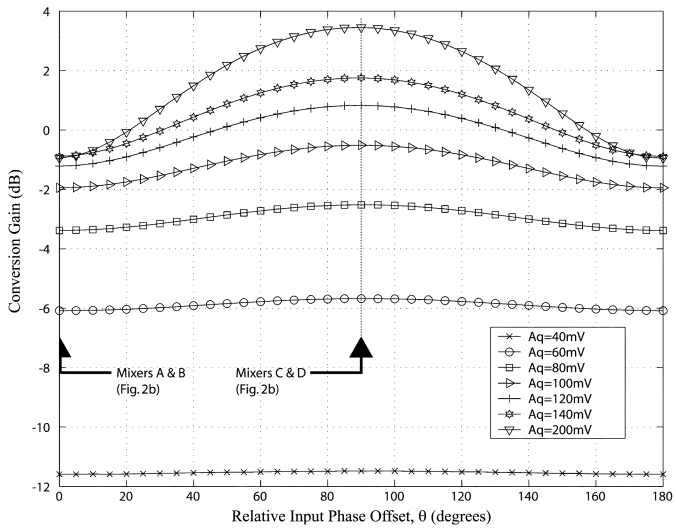

Fig. 4. Mixer conversion gain dependency on relative input phase offset.

offset.[1] When quadrature phases are required, the arrangement shown in Fig. 2(a) can be used.

The polyphase filter can be any number of stages necessary to limit the phase error variance, with returns diminishing beyond three stages and increasing phase noise with each stage added [6]. The input to the polyphase filter must have harmonic content on the order of −40 dBc or the filter outputs will be significantly unbalanced in both amplitude and phase.

In this scheme, the mixing term resulting from squaring the polyphase filters in-phase signal (mixer A) will have a DC offset, preferably removed with a tuned load to ensure matched mixer bias conditions and minimal phase error. Unfortunately, tuned loads consume die space and limit circuit bandwidth. The mixers in Fig. 2(a) also present unbalanced loads to the polyphase filter outputs, contributing to quadrature phase error.

The bulky tank circuit and unbalanced loading are addressed with the topology shown in Fig. 2(b). The $\cos(\omega t)$ and $\sin(\omega t)$ signals are output from a similar VCO-polyphase filter combination shown in Fig. 2(a). This circuit, commonly used as the IF stage in Weaver image reject mixers [7], [8], introduces considerable amplitude imbalance when mixer nonlinearities are considered. This occurs because the conversion gain of each mixer is a function of the relative phase offset of its input signals.

This effect can be shown with the simple Gilbert mixer shown in Fig. 3. The approximate large signal output of this circuit is given by [9]

$$V_{\text{out}} = \frac{R_L V_{\text{in}}}{R_E} \tanh\left(\frac{V_{\text{quad}}}{2V_T}\right) \tag{1}$$

assuming that the degeneration voltage across R_E is large in comparison to the input voltage V_{in}. Considering the topology shown in Fig. 2(b), the outputs I and Q are given by

$$I = \cos^2(\omega t) - \sin^2(\omega t) = \cos(2\omega t)$$
$$Q = 2\cos(\omega t)\sin(\omega t) = \sin(2\omega t)$$

which are in quadrature at twice the input frequency as desired.

The two inputs of mixers A and B are in-phase wheras the inputs of mixers C and D are in quadrature. When the mixer inputs are in-phase and the same frequency, the peak output occurs at the peak of the input sinusoid. At the input peak, the $\tanh(V_{\text{quad}}/(2V_T))$ term in (1) introduces compression due to

[1]Any phase offset other than $\pi/2$ will have an output DC offset, easily removed with capacitive coupling.

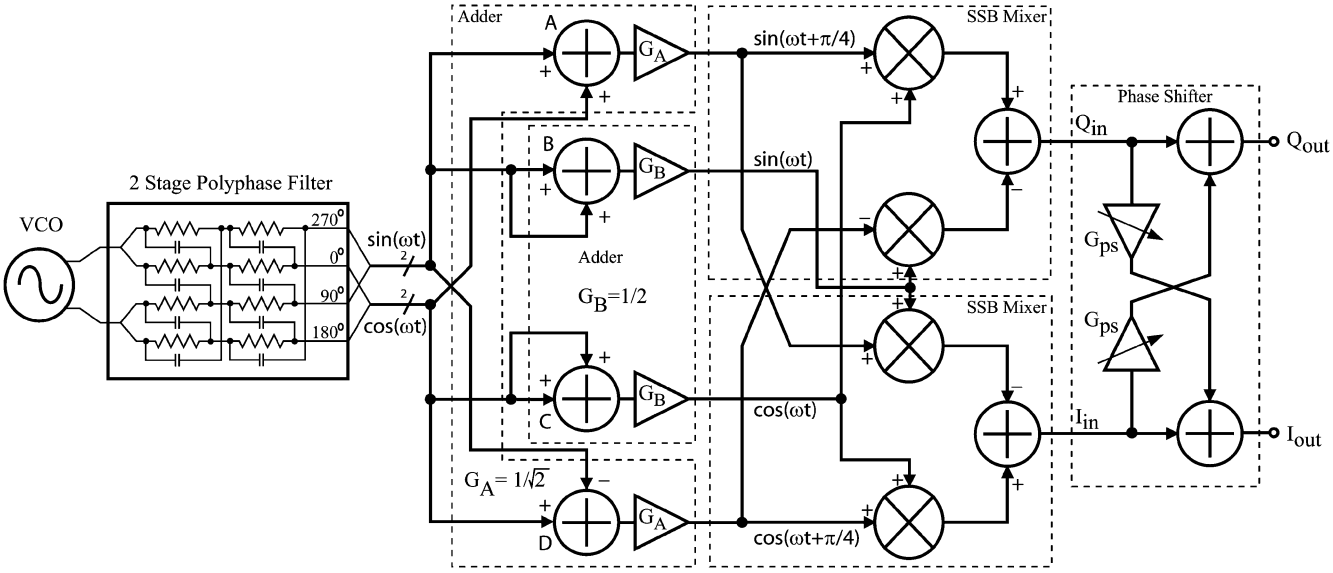

Fig. 5. Proposed frequency doubler with phase shifter.

the nonlinearity of the mixing quad devices M_1 to M_4 (Fig. 3) when $V_{\text{quad}} \gg V_T$, where V_T is the thermal voltage kT/q.

When the mixer inputs are orthogonal, the peak output occurs when the input amplitudes are at $1/\sqrt{2}$ of their peak value. The harmonics introduced by the mixing quad compression are dependent upon the input phase such that when vector summed to give the mixer output, the conversion gain will be higher for orthogonal inputs compared to when the two inputs are in-phase. The result is that the I output amplitude will be lower than the Q output, an unacceptable imbalance when used in a doubler design to provide the LO in an image reject mixer.

Fig. 4 shows the simulated conversion gain (with respect to the input port, V_{in}) of the Gilbert mixer shown in Fig. 3 as a function of the phase offset, θ, at its input ports. A_q is the peak differential drive level on the mixing quad while A_i is held constant at 100 mV. For low input levels where $A_q \ll V_T$, $\tanh(V_{\text{quad}})/(2V_T) \approx (V_{\text{quad}})/(2V_T)$ and the conversion gain shows minimal sensitivity to input phase. This implies drive levels too low to be useful for driving mixer LO ports, and subsequently a high noise floor. As A_q is increased, the conversion gain begins to saturate with respect to the quad drive level but exhibits increasing phase sensitivity. As shown, the worst case mismatch occurs when the input sinusoids are in quadrature, as used in the doubler topology shown in Fig. 2(b).

The zero crossings at each differential pair in the mixer are not affected by the mixing quad nonlinearity and hence phase error is not introduced. In practice, large signal effects in the presence of this nonlinearity will cause mixer imbalances resulting in slight phase offsets.

If the topology in Fig. 2(b), is used, the outputs will exhibit amplitude imbalance proportional to the drive level at the polyphase filter input owing to the aforementioned mixer nonlinearities. To overcome this, and zero the I/Q amplitude imbalance for any VCO input level, two approaches can be taken.

The first method attempts to linearize each mixer's conversion gain with respect to the mixer quad inputs (M_1–M_4, Fig. 3).

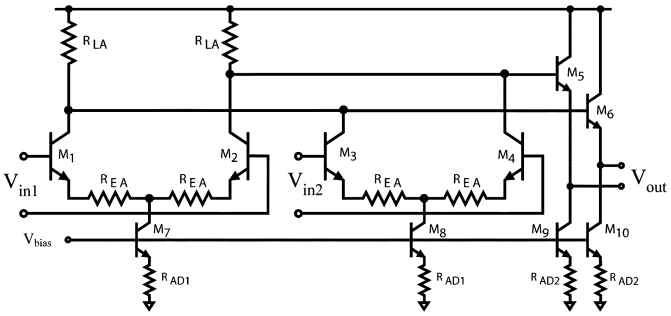

Fig. 6. Adder implementation.

This is done by predistorting V_{quad} with an exponential function, i.e., the inverse $\tanh()$ function is applied to V_{quad} in (1) to give a linear product [9]. This presupposes a wide dynamic range predistortion circuit whose process variation contributes to output phase and amplitude imbalance.

A better approach that is less sensitive to manufacturing errors is to manipulate the mixer inputs such that the relative phase at each mixer's two input ports is the same and yet still have quadrature offset in the final output signals. This is done by generating 45° phase offsets at the LO frequency and mixing them with the topology shown in Fig. 5.

Fig. 5 shows the complete proposed topology, including the phase shifter described in the following section. The load on each block output is balanced throughout. The single sideband (SSB) mixers and phase shifter blocks are drawn as single-ended connections throughout for simplicity but are implemented fully differential.

In this circuit, the VCO drives a polyphase filter to generate in-phase and quadrature signals denoted $\cos(\omega t)$ and $\sin(\omega t)$, respectively. Signal phases from 0° to 315° in 45° increments are generated in a manner similar to [10] by noting the identities

$$\cos(\omega t + \pi/4) = \frac{1}{\sqrt{2}}(\cos(\omega t) - \sin(\omega t))$$

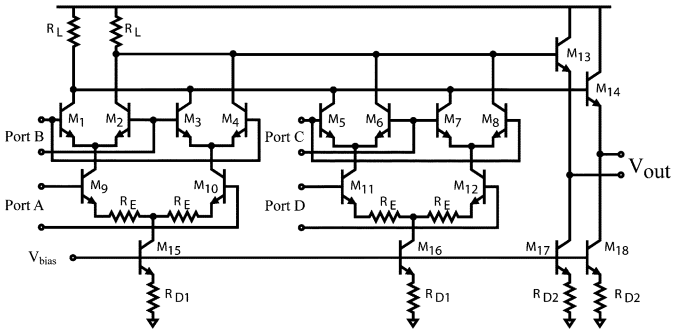

Fig. 7. Single-sideband mixer schematic.

$$\sin(\omega t+\pi/4)=\frac{1}{\sqrt{2}}(\cos(\omega t)+\sin(\omega t))$$

which gives the required phases from four adders as shown in Fig. 5. The four signal phases from the adder outputs are applied to two SSB mixers. This gives the desired double frequency outputs $I_{\rm in}$ and $Q_{\rm in}$ as

$$\begin{aligned} I_{\rm in} &= \cos(\omega t)\cos(\omega t+\pi/4)-\sin(\omega t)\sin(\omega t+\pi/4)\\ &= \frac{\sqrt{2}}{2}(\cos(2\omega t)-\sin(2\omega t))\\ Q_{\rm in} &= \cos(\omega t)\sin(\omega t+\pi/4)+\sin(\omega t)\cos(\omega t+\pi/4)\\ &= \frac{\sqrt{2}}{2}(\cos(2\omega t)+\sin(2\omega t)) \end{aligned}$$

which are in quadrature with equal amplitude outputs. Note that by introducing $\pi/4$ phase increments, each mixer in Fig. 5 has its two inputs at the same relative phase offset, thereby matching the mixer nonlinearity effects in both the in-phase and quadrature paths.

The adder schematic is given in Fig. 6 with the gain G_A, G_B given in Fig. 5 set via the ratio R_{LA}/R_{EA}. Values for G_A and G_B listed in Fig. 5 are as required from first-order analysis. More adder gain is necessary when implementation loss is considered. The load R_{LA} must be the same for all four adders and the ratio is set by choosing R_{EA} as required. This minimizes the variation in adder phase shift due to the RC filter formed by the load resistors and parasitic output capacitances.

To ensure a balanced load on the polyphase filter and to match the delays through the adders, the 0° and 90° phases are generated by adding the corresponding polyphase signals to themselves and scaling the sum and difference terms by 1/2. Generating $\cos(\omega t)$ and $\sin(\omega t)$ in this way adds a seemingly redundant pair of adders (B and C, Fig. 5) but is necessary to match the delays introduced by adders A and D.

Fig. 7 shows the schematic for each of the SSB mixers shown in Fig. 5. A tuned load is not required since the input signal phases are such that no DC offset will be output. Ports A to D are biased with four separate high-pass RC filter networks. Although the adder outputs will have a common-mode level suitable to drive ports A and D in Fig. 7, ports B and C require level shifting to a higher voltage. Any level shifter will introduce a phase shift that must be matched at ports A and D. Alternatively, two sets of followers, one for each common-mode level required, could be used at the expense of power consumption and increased common-mode voltage mismatch.

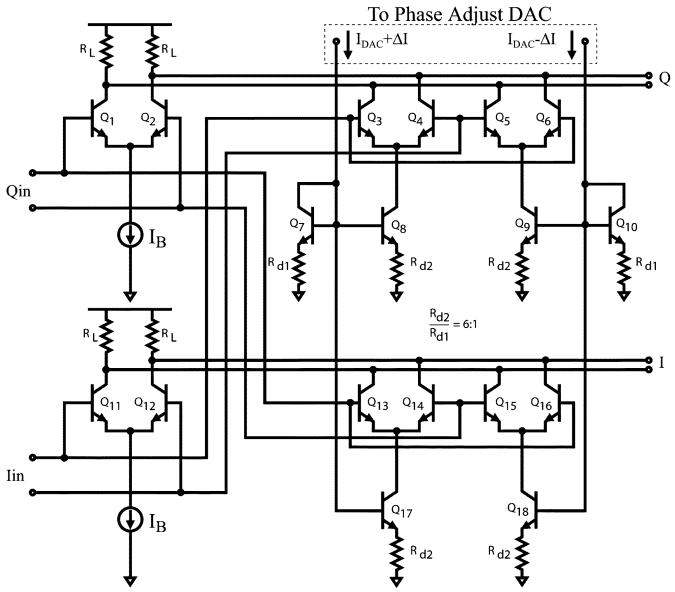

Fig. 8. Phase shifter schematic.

The polyphase filter is the largest source of phase error. Lower phase error variations can be achieved if a quadrature VCO topology is used [11], [12]. The consequence of using a quadrature VCO is an additional resonant tank circuit and regenerative cell. The additional VCO power required is offset by the reduced output level required when the polyphase filter, and its inherent losses, is removed.

B. Phase Shifter

The phase shifter is connected in cascade with the SSB mixers as shown in Fig. 5. With careful layout, the typical quadrature output phase error will be $\ll 1^\circ$ and some means of achieving programmable phase shifts on the order of $\pm 5^\circ$ are required to compensate for phase error changes due to device mismatch as well as variations in process, temperature, and supply voltage.

The desired phase shifter outputs can be written as

$$I=\cos\left(\omega t+\frac{\theta}{2}\right)=\cos(\omega t)\cos\left(\frac{\theta}{2}\right)-\sin(\omega t)\sin\left(\frac{\theta}{2}\right) \quad (2)$$

$$Q=\sin\left(\omega t-\frac{\theta}{2}\right)=\sin(\omega t)\cos\left(\frac{\theta}{2}\right)-\cos(\omega t)\sin\left(\frac{\theta}{2}\right) \quad (3)$$

where θ is the variable phase shift to be introduced. If the assumptions $\sin(x)\approx x$ and $\cos(x)\approx 1$ for $x<0.1$ are made, (2) and (3) can be simplified to

$$I=\cos(\omega t)-\sin(\omega t)\left(\frac{\theta}{2}\right)\approx\cos\left(\omega t+\frac{\theta}{2}\right) \quad (4)$$

$$Q=\sin(\omega t)-\cos(\omega t)\left(\frac{\theta}{2}\right)\approx\sin\left(\omega t-\frac{\theta}{2}\right) \quad (5)$$

and hence the phase shift θ can be introduced by adding a fraction, proportional to the desired phase shift, of the in-phase signal to the quadrature signal and *vice versa*. Introducing programmable phase shift is accomplished by changing the fraction of the cross-coupled signal. It is important that the cross-coupled signals added undergo the same delay to keep the above assumption valid.

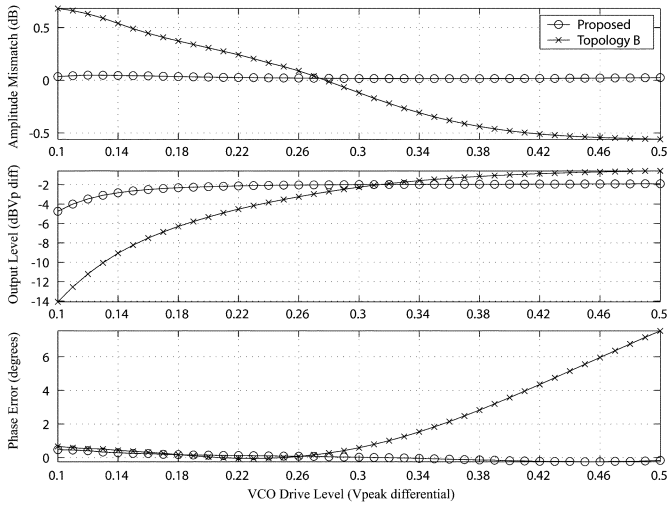

Fig. 9. Simulated input amplitude sensitivity of topology in Fig. 2(b) (topology B) in comparison to the proposed design.

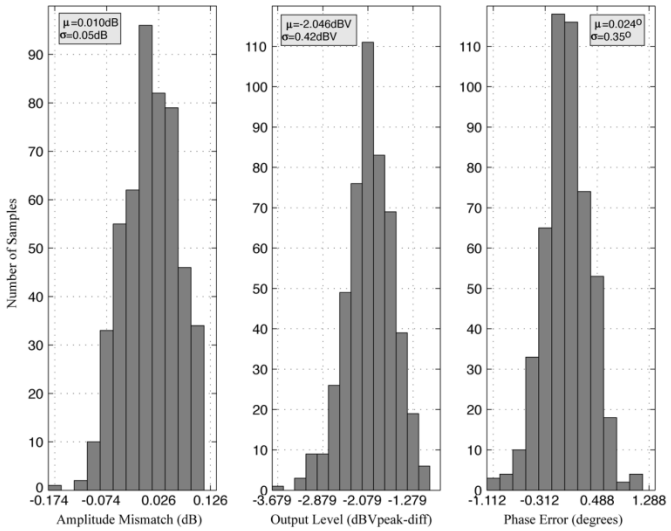

Fig. 10. Monte Carlo simulations of phase and amplitude imbalance (500 runs).

Introducing the phase shift in this way allows the phase shifter to apply gain to the input signals and is amenable to automatic level control when implemented as shown in Fig. 8. Analog phase control can alternatively be used by steering continuous currents into mirror devices Q_7 and Q_{10}. Digital control was implemented with a static 5-bit current-steering DAC to give binary weighted currents, ΔI, added to a constant bias current I_{DAC} in Fig. 8.

The phase tuning range is determined by the ratio of quadrature signal added to each feedforward path, i.e., G_{ps} in Fig. 5. The gain of the phase shifter can be varied by changing the bias current I_B in Fig. 8. The same phase tuning range can then be restored by proportionally changing the full-scale DAC current ΔI.

A small phase step and adequate range is desirable if the doubler is used to provide the LO for an SSB mixer. If the tuning range is too wide and discrete steps are used, the reciprocal dependence of the mixer sideband rejection on phase error can considerably lower the average achievable sideband rejection. This can be overcome with analog phase control or a more flexible DAC with selectable reference currents.

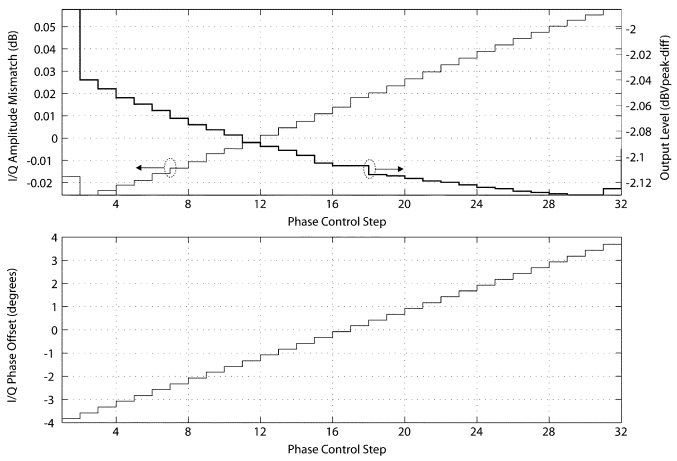

Fig. 11. Simulated programmable quadrature phase offset steps.

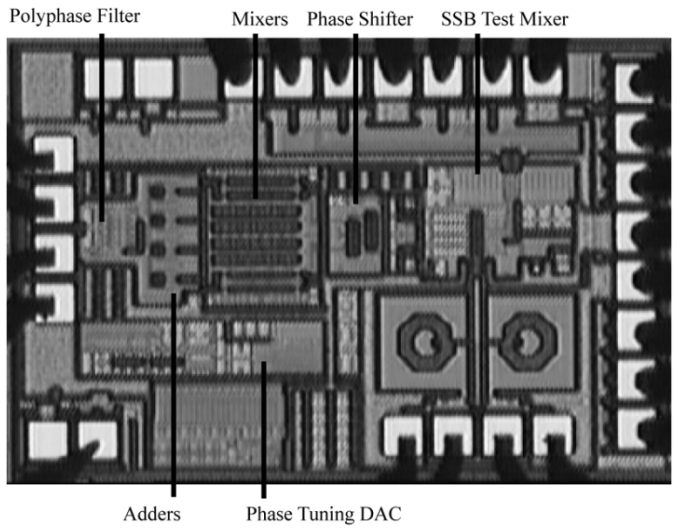

Fig. 12. Die photo of frequency doubler and single sideband mixer.

The phase shifter is the dominant source of amplitude variation and harmonic distortion owing to the nonlinear input pairs Q_1, Q_2, and Q_{11}, Q_{12}. If a constant output level is desired, or, level control is implemented in another block, these input pairs may be degenerated to reduce the distortion added. This, however, requires a large increase in ΔI to compensate for the reduced gain of the linearized input pair.

III. Performance

A. Simulation

Fig. 9 shows the quadrature phase and amplitude balance immunity to input amplitude variations offered by the proposed topology. The circuit in Fig. 2(b) has only a single input level at which the output I/Q amplitudes are balanced and hence use of this doubler requires strict control of the input LO amplitude. Similarly, the phase error of the circuit in Fig. 2(b) increases proportional to the input level as the amplitude is increased beyond 250 mV.

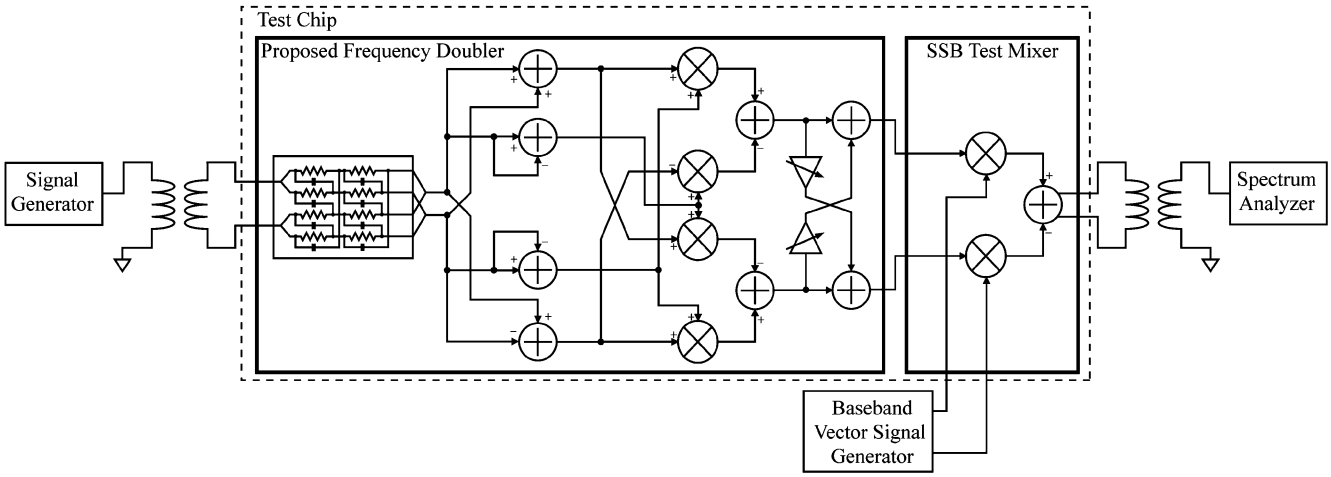

Fig. 13. Test chip to demonstrate the proposed frequency doubler.

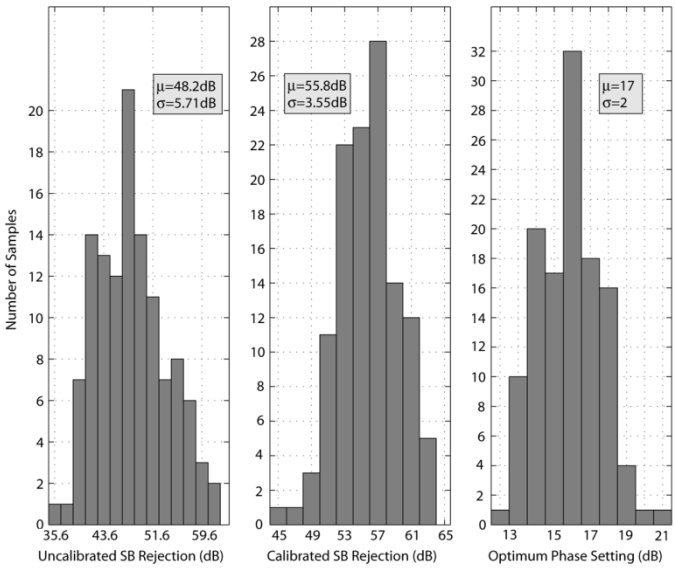

Fig. 14. Measured mixer sideband rejection.

The effect of process variation and device mismatch is shown with Monte Carlo simulation in Fig. 10 with the average, μ, and standard deviations, σ, as indicated in the plots. The programmable phase steps are shown in Fig. 11 as the 5-bit control word is varied over each of 32 possible states. A linear stepped tuning range of $\approx\pm 4^{\circ}$ is realized with negligible effect on the amplitude imbalance and a <0.2 dB change in the overall output I/Q level.

B. Measurement

The die photo of the frequency doubler with the SSB test mixer is shown in Fig. 12. The schematic of this chip, shown in Fig. 13, uses an SSB upconversion mixer whose LO inputs are driven by the proposed doubler. The LO input and differential I/Q baseband inputs are provided by an external signal generator and vector signal generator, respectively.

The design was implemented in a 0.32 μm SiGe BiCMOS process. The doubler can operate over a 3–3.6 V supply voltage in an ambient temperature range of -20°C to $+85^{\circ}$C. Measurement results given were done for 60 parts sampled evenly across

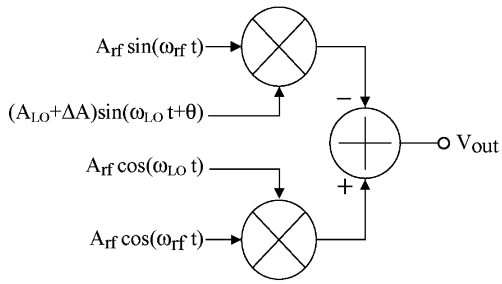

Fig. 15. Quadrature errors in SSB mixer.

a single wafer. A nominal supply voltage of 3.3 V with RF input frequencies from 4.9 GHz to 6 GHz were used for all measurements. The baseband input frequency was fixed at 30 MHz at a 100 $\mathrm{mV_{RMS}}$ differential input level, well within the test mixer's linear input range.

Fig. 14(a) shows the measured sideband rejection of the test circuit given in Fig. 13 before phase correction is applied. The data shown corresponds to 120 sample points for 60 devices at each supply voltage corner of 3 V and 3.6 V. The low nominal phase and amplitude errors of the doubler result in an average sideband rejection of 48.2 dB with a standard deviation, σ, of 5.71 dB. This corresponds to a simulated average sideband rejection and σ of 53 dB and 5.6 dB, respectively. When the phase offset is optimized, these measures improve to 55.8 dB and 3.55 dB as shown in Fig. 14(b).

The optimum phase setting plot in Fig. 14(c) is the DAC step out of a possible 32 that resulted in the highest sideband rejection. A setting of 16 gives no phase offset, 1 gives maximum negative phase and 32 the maximum positive phase offset. A phase offset of 1 standard deviation corresponds to $\approx\pm 0.3^{\circ}$ of phase shift required to restore LO quadrature. This indicates a low uncalibrated nominal phase error in the topology proposed.

The device mismatch and layout asymmetries in the test mixer will contribute to the sideband rejection measured. These effects are indistinguishable from the quadrature errors of the frequency doubler. Similarly when measuring spurious outputs, the LO leakage due to the input referred DC offset of the test mixer will be superimposed upon the leakage component of the doubler.

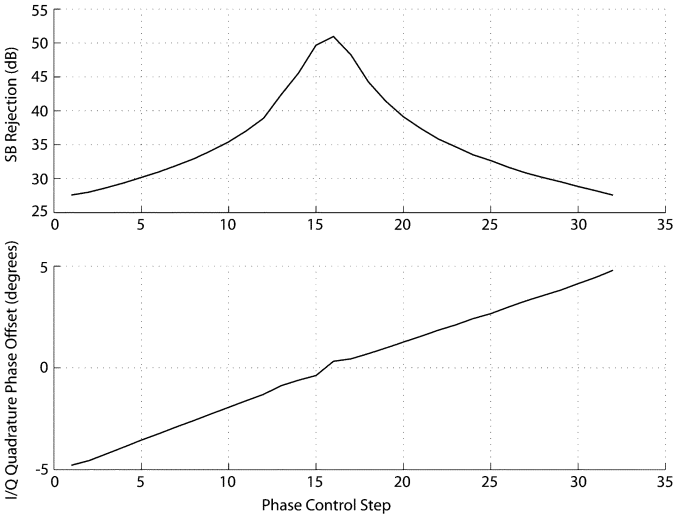

Fig. 16. Measured sideband rejection as a function of phase tuning with corresponding inferred quadrature phase offset.

Direct measurement of phase offset is difficult at the frequencies considered. However, the phase error can be inferred from sideband rejection measurements made on the SSB test mixer. With reference to Fig. 15, if the doubler output signal has an I/Q amplitude imbalance of ΔA and phase error of θ, the sideband rejection (SBR) in dBc is given as

$$\mathrm{SBR} = 10\log\left(\frac{\left[1-\left(1+\frac{\Delta A}{A}\right)\cos\theta\right]^2+\sin^2\theta}{(1+\cos\theta)^2+\sin^2\theta}\right). \quad (6)$$

For sufficiently high VCO drive levels, the doubler outputs will amplitude limit. This causes the sideband rejection to be largely determined by the phase error and hence (6) can be approximated as

$$\mathrm{SBR} \approx 10\log\left(\frac{(1-\cos\theta)^2+\sin^2\theta}{(1+\cos\theta)^2+\sin^2\theta}\right) \quad (7)$$

which can be solved for θ as the sideband output power is swept via the phase offset control. Fig. 16 shows the nominal measured sideband rejection for each setting of the phase control word and the LO quadrature phase error inferred from (7), yielding an approximate tuning range of -5° to $+5^\circ$.

Fig. 17 shows both the calibrated and uncalibrated sideband rejection as the doubler LO input power is swept. As shown, the architecture shows low sideband rejection sensitivity to the input power level. This reduced input amplitude sensitivity occurs despite the mixers in the doubler circuit being driven beyond their linear range as a result of using matched 45° phase offsets to drive each mixer.

For low input levels, no stages in the doubler are amplitude limited and hence both amplitude and phase errors contribute to lower sideband rejection. As the input amplitude increases, amplitude limiting lowers the amplitude mismatch leaving only phase imbalance and improved sideband rejection. For very high input levels approaching $+6$ dBm, mixer nonlinearities begin to limit the achievable sideband rejection as shown in Fig. 17.

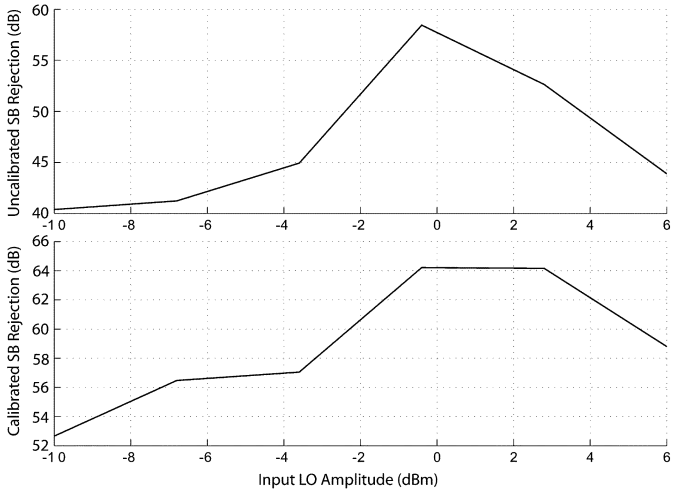

Fig. 17. Sideband rejection sensitivity to input power.

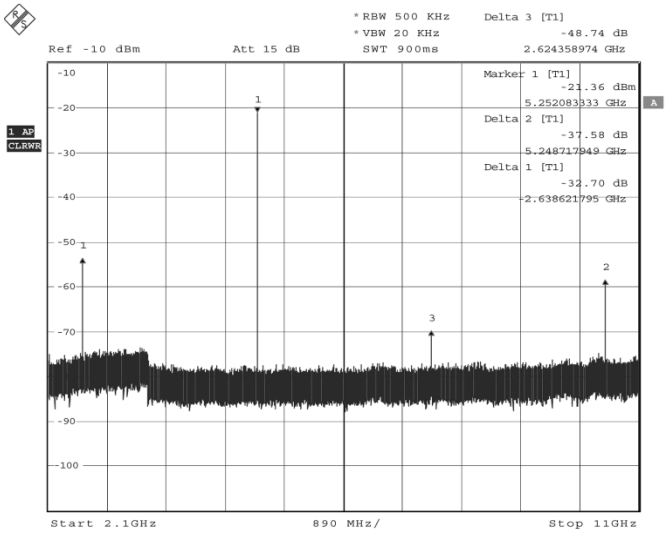

Fig. 18. Frequency doubler output spectrum.

The output spectrum of the doubler, showing spurious content is shown in Fig. 18. The measured output level is low due to the wafer probe configuration, cable and balun losses at both input and output and the 50 Ω output load. The doubler was designed to take a 200 mVp differential input from a VCO and output 200 mVp to 300 mVp differential for capacitive loads on the order of 100 fF.

Nominal supply, 5.25 GHz output frequency, and a high drive level of $+6$ dBm were used. The largest spur is the direct feed through of the input LO signal at -32.7 dBc. This can be removed with a DC offset correction at the mixer inputs if provisions are made to do so. The third and fourth harmonics of the LO are below -37 dBc and improve dramatically as the input level is backed off from the $+6$ dBm drive level used.

Fig. 19 shows the output spectrum of the doubler driven by a signal generator at 2.625 GHz. The output phase noise density is 6 dB above the input phase noise density for all frequency offsets where the output level is above the noise floor of the measurement system (offset <100 kHz). The spurs at approximately

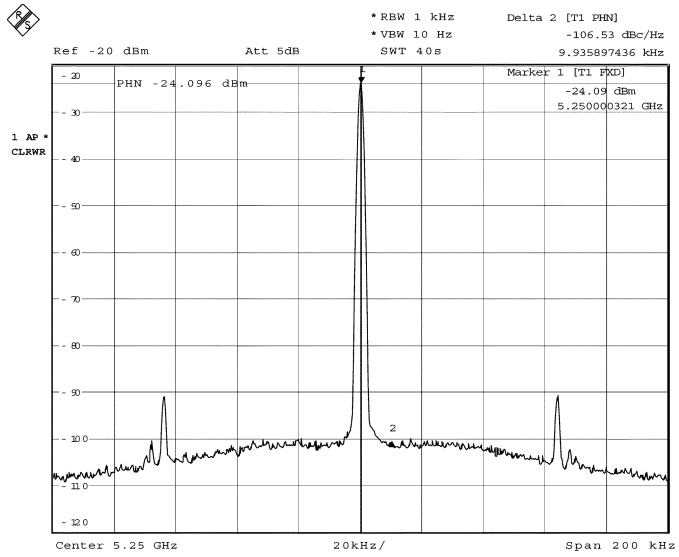

Fig. 19. Frequency doubler output phase noise.

62 kHz offset are comparison spurs from the input signal generator's synthesizer.

Each adder draws 4 mA with an additional 4 mA used to buffer its outputs. The SSB mixers draw a combined current of 12 mA with 4 mA used for buffers. The phase shifter draws a total of 5 mA and the final output buffers use a combined current of 8 mA. All bias cells consume a total current of 2.8 mA.

This gives a total 33 mA current in the core doubler circuit with an additional 28 mA used for buffering to drive the low impedance loads of the test circuit. Typically the doubler will not be required to drive 50 Ω loads and hence the power spent on buffering for the test cell can be significantly reduced.

The doubler was developed for a multi-channel WLAN access point [1] where power consumption was traded off for high drive capability and lower nominal phase error. The intent of this was to reduce the need to calibrate the phase offset. If power consumption is a concern and the phase correction will be used, significant power savings can be made by allowing an increase in the phase error variance and subsequently correcting the offset with the phase control.

IV. Conclusion

A broadband frequency doubler circuit has been proposed and verified with measurements. Low quadrature phase and amplitude error has been shown with an SSB mixer that achieves 48.2 dB average sideband rejection and 55.8 dB after optimization of the output phase offset. The input polyphase filter is the only frequency selective block in the circuit and is all that needs to be changed to allow the doubler to be used over different frequency ranges.

The proposed design exhibits low sensitivity to process, supply voltage and temperature variations and is suitable for manufacture in volume. The architecture makes use of common circuits typically available or readily designed.

The topology is not limited to implementation with bipolar devices and is amenable to design in bulk CMOS without additional thick metal layers since spiral inductors are not used.

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References

[1] "Wideband Multi-Channel Wireless LAN Chipsets for Next Generation Access Points," Engim, Inc., Acton, MA, White Paper, 2002.

[2] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1415–1424, Sep. 2004.

[3] A. Chung and J. Long, "A 5–6-GHz bipolar quadrature-phase generator," *IEEE J. Solid-State Circuits*, vol. 39, no. 10, pp. 1737–1745, Oct. 2004.

[4] J. Maligeorgos and J. Long, "A low-voltage 5.1–5.8-GHz image-reject receiver with wide dynamic range," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1917–1926, Dec. 2000.

[5] T. Tsukahara and J. Yamada, "3 to 5 GHz quadrature modulator and demodulator using a wide-band frequency-doubling phase shifter," in *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, Feb. 2000, pp. 384–385.

[6] F. Behbahani, Y. Kishigami, J. Leete, and A. Abidi, "CMOS mixers and polyphase filters for large image rejection," *IEEE J. Solid-State Circuits*, vol. 36, no. 6, pp. 873–887, Jun. 2001.

[7] J. C. Rudell, J.-J. Ou, T. B. Cho, G. Chien, F. Brianti, J. A. Weldon, and P. R. Gray, "A 1.9-GHz wide-band IF double conversion CMOS receiver for cordless telephone applications," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 2071–2088, Dec. 1997.

[8] B. Razavi, *Microelectronics*. Upper Saddle River, NJ: Prentice-Hall, 1998.

[9] A. B. Grebene, *Bipolar and MOS Analog Integrated Circuit Design*. New York: Wiley, 1984.

[10] K. Koh, M. Park, C. Kim, and H. Yu, "Subharmonically pumped CMOS frequency conversion (up and down) circuits for 2-GHz WCDMA direct-conversion transceivers," *IEEE J. Solid-State Circuits*, vol. 39, no. 6, pp. 871–884, Jun. 2004.

[11] M. Tiebout, "Low-power low-phase-noise differentially tuned quadrature VCO design in standard CMOS," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1018–1024, Jul. 2001.

[12] P. Andreani, A. Bonfanti, L. Romano, and C. Samori, "Analysis and design of a 1.8-GHz CMOS LC quadrature VCO," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1737–1747, Dec. 2002.

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