Monolithic Tunable Active Inductor with Independent Q Control

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***Abstract*—A 1.1-GHz fully integrated GaAs MESFET active inductor is presented in this paper. Both the inductance and loss resistance are tunable with the inductance independent of series loss tuning. The measured loss resistance is tunable over a −10- to +15-Ω range with a corresponding change in inductance of less than 10% at 100 MHz and less than 4% for frequencies above 500 MHz. The inductance is tunable from 65 to 90 nH. Considerably larger bandwidths can be achieved depending on the fabrication technology employed and the intended application of the circuit.**

***Index Terms*—Active inductor, GaAs, MESFET, MMIC, tunable.**

I. Introduction

A SIGNIFICANT restraint in monolithic-microwave integrated-circuit (MMIC) design stems from the difficulty in realizing an integrated passive inductor with sufficiently high Q over a broad bandwidth. Large space requirements, low inductance values, and low Q factors make these inductors unsuitable for precision applications.

Active designs have allowed larger inductance values to be realized. However, the active inductors published to date are limited in that they are often not tunable. When inductance tuning is introduced, the Q factor usually shows a strong dependence on both the tuning parameter and frequency of operation. As a result, tuning both the inductance and the Q factor requires an iterative tuning procedure.

One of the most notable Q-enhancing techniques has been described by Tokumitsu *et al.* in [1]. In this design, a cascode FET arrangement with resistive feedback is used such that when the FET's are matched, the active inductor's loss resistance can be canceled. The resistive feedback described in [1] was replaced with a common-gate FET in [2], which offered improved Q factor. However, tuning of Q or the inductance was not easily accomplished.

Alinikula *et al.* [3], [4] described an alternative topology to that given in [2], which offered greater tuning flexibility. With this technique, the effect of finite channel conductance $g_{\rm ds}$ was examined and a design was proposed that minimized sensitivity to $g_{\rm ds}$. Using an FET operating in its linear region as a variable resistor, the frequency at which maximum Q occurred could be controlled. For narrow bandwidths, the Q factor approached 500, however, the loss resistance showed a strong frequency dependence.

A novel resonator design described by Haigh [5] introduced tuning of both the resonant frequency and the Q factor. A resonant circuit was formed by using two integrators terminated in a capacitance and connected in a feedback loop. Although the resonant frequency remained independent of Q tuning, the circuit showed a large loss resistance for frequencies below the resonant frequency.

Tuning control of both inductance and Q factor was also reported in a novel topology proposed by Lucyszyn and Robertson [6]. This design simulated an inductance that was adjustable over a narrow range of values by changing the gate bias voltage of a single FET. The Q factor could also be tuned to be maximum at an arbitrary frequency. However, as with the previous design, the loss resistance showed an appreciable frequency dependence resulting in very narrow-band performance.

A more recent design presented by Yong-Ho *et al.* [7] expanded on a common Q enhancement technique using a single FET with lossy inductive feedback. Instead of using a passive feedback inductor, an active inductor circuit was used in this design. The inductance was made tunable over a wide range by varying the loss resistance of the active feedback circuit. Tuning of the Q factor was accomplished by varying the positive supply voltage for all FET's and could only be set to infinity for a narrow band of frequencies. The loss resistance also varied over a wide range for frequencies outside of this narrow band.

Sussman–Fort *et al.* [8] proposed a unique compensation technique to realize a gyrator with reduced parasitic effects by replacing the terminating impedance with a passive *RLC* network. Simulation results confirmed circuit operation as an active inductor over a frequency range from 1 to 3 GHz; however, the passive *RLC* network needed to terminate the gyrator is difficult to fully integrate given the high tolerance of passive components on chip. This is further complicated by the need for passive inductors in the terminating impedance, which introduce significant parasitics, thus requiring an iterative procedure to design the gyrator's passive load.

Several techniques using active compensation of lossy passive structures were proposed in separate works by Brucher *et al.* and Sussman–Fort [9], [10] for use in microwave filters. Although these design methods allowed high-Q filters to be realized, many of these techniques were difficult to realize in monolithic form or did not allow the synthesis of a pure inductance for use in other high-frequency applications that require a purely inductive impedance.

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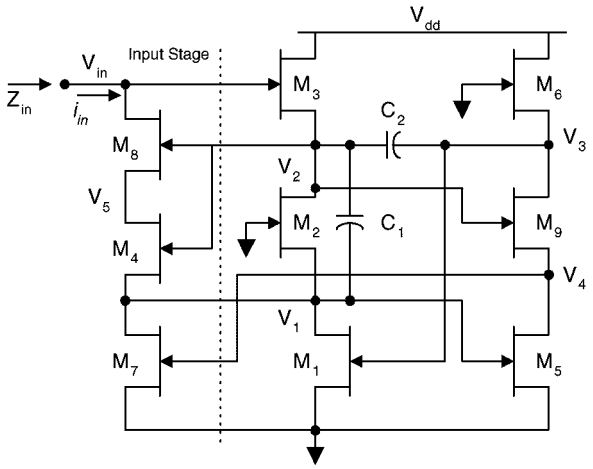

Fig. 1. Active inductor schematic without dc-bias components.

Recently, Sinsky *et al.* [11] presented simulation results for a negative capacitance circuit using conventional second–generation current conveyor design techniques. Tunability of the synthesized impedance could be introduced by replacing resistors in each circuit with an FET biased to give a variable resistance. Each current conveyor was implemented as several cascaded MESFET's such that the equivalent FET had significantly higher gain, thus approaching more ideal behavior of a current conveyor. In order to get sufficiently high gain, however, each current conveyor required large FET's with gatewidths of the order of 600 μm, and two current conveyors were required in addition to off chip biasing components.

A thorough review of many classical two- and three-transistor active inductor circuits in addition to several new topologies has been given by El Khoury [12]. From first-order analysis, these circuits are capable of realizing both positive and negative floating inductance values, but all are limited in their tunability and exhibit many undesirable effects resulting from FET parasitics.

In this paper, an alternative design is presented with more flexible tuning control. With this new technique, the series loss resistance of the simulated inductance is frequency independent over a wide bandwidth. This constant resistance can be varied over a broad range of both positive and negative values with negligible impact on the effective inductance of the circuit. The inductance realized by the circuit is also tunable and remains independent of series loss tuning.

II. Design and Analysis

A. Circuit Design

The schematic of the new active inductor is shown in Fig. 1. Both the simulated inductance $L_{\rm eq}$ and the series loss resistance $R_{\rm loss}$ are made tunable with two variable capacitors C_1 and C_2. If $R_{\rm loss}$ is to be tunable independently of the inductance, the input impedance expression must be of the form

$$Z_{\rm in} = j\omega L_{\rm eq}(C_1) + R_{\rm loss}(C_1, C_2) \tag{1}$$

which consists of an inductance and a frequency-independent series resistance that are some function of the tuning capacitors C_1 and C_2. The input impedance will depend primarily on C_1 and C_2 provided they are much larger than the FET parasitic capacitances. This allows the two capacitors C_1 and C_2, shown in Fig. 1, to be used for tuning of $L_{\rm eq}$ and $R_{\rm loss}$ where $R_{\rm loss}$ can be controlled by C_2 and $L_{\rm eq}$ can be independently controlled by varying C_1 while keeping the ratio C_1/C_2 constant.

The circuit can be treated as two independent stages consisting of a voltage-to-current conversion at the input and a six-FET frequency-dependent voltage generator, as shown in Fig. 1. The circuit behaves as a gyrator with a tunable series loss resistance where C_1 is the terminating load whose impedance is to be inverted.

In order to realize an ideal gyrator, the small-signal input current $i_{\rm in}$ must be proportional to the product of the port voltage $v_{\rm in}$ and the terminating load impedance $1/(j\omega C_1)$. Realizing such a circuit is simplified if a small-signal voltage can be generated that is proportional to the load impedance and is a linear function of $v_{\rm in}$. This allows $i_{\rm in}$ to be set as required with a simple voltage to current conversion. For the circuit in Fig. 1, the necessary frequency-dependent voltages are given by V_1 and V_2. The difference $V_2 - V_1$ is then converted to a proportional current by the input stage to set $i_{\rm in}$ as required.

With M_1, M_2, and M_3 in a common-source cascode topology, V_1 and V_2 (shown in Fig. 1) are generated such that if the current into the input port $i_{\rm in}$ is set proportional to V_1 or V_2, both $L_{\rm eq}$ and $R_{\rm loss}$ will depend on both C_1 and C_2.

Independence of the inductance from $R_{\rm loss}$ can only be achieved provided $L_{\rm eq}$ does not depend on both C_1 and C_2. This is accomplished with a second cascode arrangement consisting of M_5, M_6, and M_9 used to form a feedback loop. This sets the gate voltage of M_1 to V_3, which is a phase-shifted version of V_1, causing the transfer functions from the input to V_1 and V_2 to have the same poles.

The input stage formed by M_7, M_4, and M_8 forms a voltage-to-current conversion that sets the input impedance $Z_{\rm in}$ inversely proportional to $V_2 - V_1$. M_4 sets the small-signal input current equal to $g_{m4}(V_2 - V_1)$, resulting in an input impedance with resistive and inductive terms only and with the required form given in (1). FET M_9 has no effect on the feedback voltage V_3 and is only required to set the drain current of M_7 to $g_{m4}(V_2 - V_1)$, provided M_7 and M_4 are matched. If M_7 and M_4 are matched, then the voltage-to-current conversion given by M_7, M_4, and M_8 has no impact on node voltages V_1 or V_2 since M_4 injects a current into node V_1 equal to that pulled from the node by M_7.

FET's M_7 and M_8 are included to reduce the sensitivity of $Z_{\rm in}$ to the high channel conductance of the input stage FET's. Alternative stacked FET arrangements can be used to minimize the effects of $g_{\rm ds4}$ and $g_{\rm ds8}$. However, the proposed topology reduces the number of FET's required, as well as minimizes the effects of M_4's capacitive parasitics.

B. Circuit Analysis

From Fig. 1, $Z_{\rm in}$ can be found from straightforward nodal analysis. Small-signal analysis of the circuit gives V_1 and V_2 as

$$V_1 = \frac{g_{m3}V_{\rm in}(C_1 g_{m5} - g_{m2}C_2 + j\omega C_1 C_2)}{Aj\omega + B} \tag{2}$$

$$V_2 = \frac{g_{m3}V_{\text{in}}(C_1 g_{m5} + g_{m2}C_2 + j\omega C_1 C_2)}{Aj\omega + B} \tag{3}$$

where

$$A = C_1 C_2(g_{m2} + g_{m3} + 2g_{m5})$$
$$B = C_2(g_{m2}^2 + g_{m2}g_{m3}) + C_1(g_{m5}g_{m3} - g_{m5}g_{m2})$$

assuming that C_1 and C_2 are much larger than the parasitic capacitances of each FET. Both V_1 and V_2 are first-order functions of the input port voltage V_{in}.

The feedback voltage V_3 causes (2) and (3) to differ only by a sign inverted coefficient in their numerator terms. By subtracting V_1 from V_2, only a single constant term remains in the numerator expressions, completely removing the inductor's dependence on C_2. Setting the small-signal input current equal to $g_{m4}(V_2 - V_1)$, the equivalent inductance of the circuit L_{eq} is given by

$$L_{\text{eq}} = C_1 \frac{g_{m2} + g_{m3} + 2g_{m5}}{2g_{m2}g_{m3}g_{m4}} \tag{4}$$

which is tunable via C_1 with a series loss resistance given by

$$R_{\text{loss}} = \frac{g_{m2}^2 + g_{m2}g_{m3}}{2g_{m2}g_{m3}g_{m4}} + \frac{KC_1}{C_2} g_{m5}\left(\frac{g_{m3} - g_{m2}}{2g_{m2}g_{m3}g_{m4}}\right) \tag{5}$$

which is frequency independent and tunable via C_2. K is a dimensionless curve-fitting constant where $0.3 < K < 0.4$. This parameter allows the effects of the large FET channel conductances to be modeled without complicating the expression for R_{loss}. Solving for R_{loss} using V_1 and V_2, given in (2) and (3), respectively, results in (5) with $K = 1$. Simulation and measurement, however, have shown that the collective effect of parasitics can be accurately modeled with a smaller value of K since the effect of parasitics is to change the value of R_{loss} for a given value of C_2, but the tuning range of R_{loss} is not altered.

For an appropriate choice of FET dimensions, R_{loss} can be made tunable over a wide range of both positive and negative resistances. Since (4) is independent of C_2, the simulated inductance is independent of series resistance tuning. R_{loss} will also be independent of L_{eq} tuning provided the ratio C_1/C_2 is held constant as C_1 is varied.

III. Realization and Performance

The layout of the active inductor is shown in Fig. 2. A 1-μm GaAs MESFET process was used resulting in a total chip area of 1.2 mm × 1.7 mm for the complete circuit. The test chip was wire bonded to a chip carrier and the input impedance measurements were done with an HP8510C Network Analyzer interfaced through an Elite Test jig.

In order to test the fabricated design, both the inductance and Q tuning capacitors were built as an array of metal–insulator–metal (MIM) capacitors, which, when connected in parallel, resulted in a capacitance value for C_2 larger than that required for an infinite Q factor and C_1 set to its largest value. When tuning the input impedance, each capacitor was then reduced in small increments by progressively breaking air bridges supporting the second metal layer between each sub-capacitor, effectively removing it from the parallel connection. As C_2 was decreased, R_{loss} decreased in accordance with (5), eventually becoming negative. Similarly, as C_1 was decreased, L_{eq} decreased.

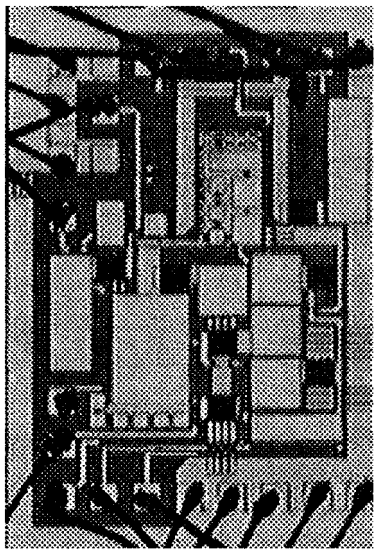

Fig. 2. Die photograph of active inductor. Total area is 1.2 mm × 1.7 mm.

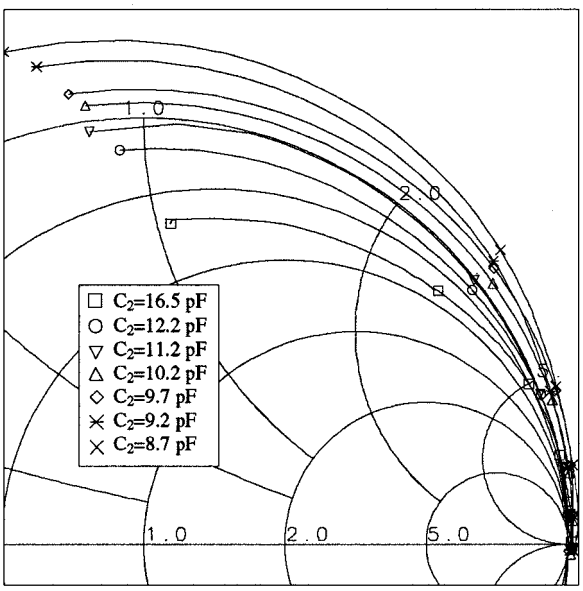

Fig. 3. Measured effect of varying the Q tuning capacitor C_2 (0.1 GHz $< f <$ 1 GHz).

With C_1 fixed to give a constant inductance, C_2 was lowered in small decrements, resulting in the set of impedance plots shown in Fig. 3. The initial value of C_2 caused the first impedance measured to have a large positive loss resistance ($+15\ \Omega$), as predicted by (5). Decreasing C_2 increased the Q factor, until a sufficiently low loss was realized, as shown in Fig. 3. The simulation results corresponding to the same tuning conditions are shown in Fig. 4.

Continuing to lower C_2 beyond this point made the series loss resistance negative in accordance with (5). The wide loss resistance tuning range is shown in Fig. 5 in comparison to the expected values from both simulation and (5). R_{loss} can be tuned

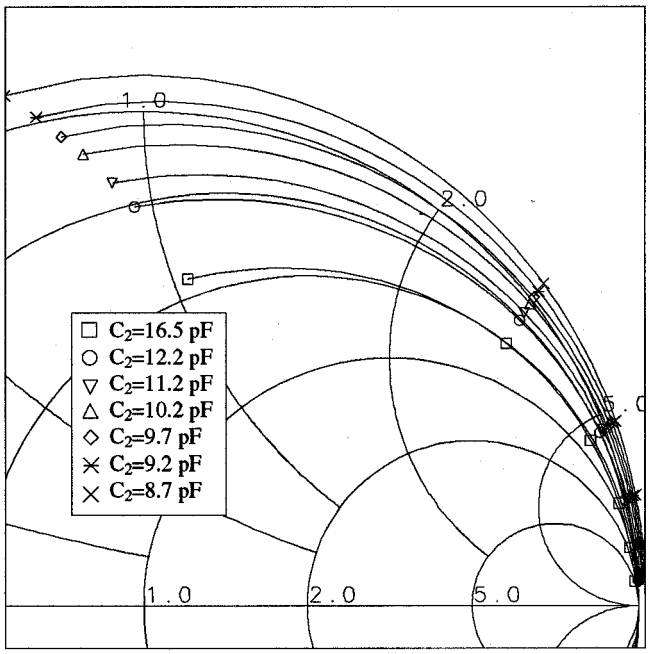

Fig. 4. Simulated effect of varying the Q tuning capacitor C_2 (0.1 GHz $< f <$ 1 GHz).

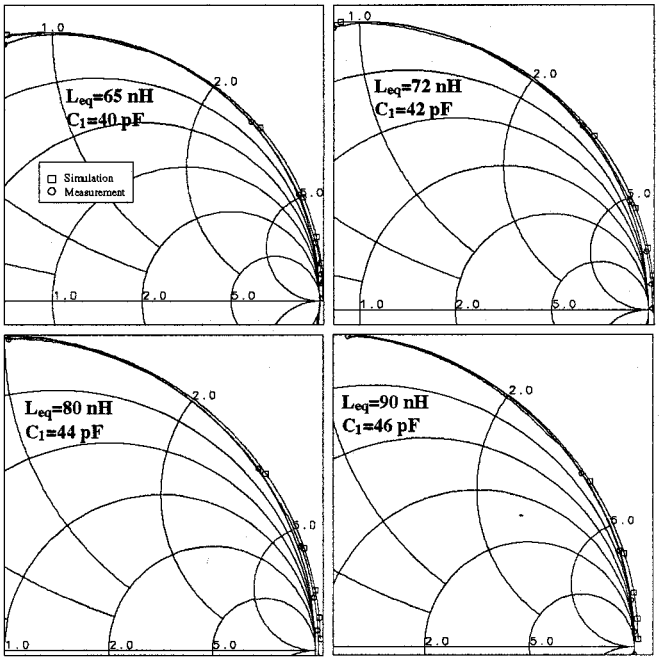

Fig. 6. Simulated and measured effect of varying the inductance tuning capacitor C_1 (0.1 GHz $< f <$ 1 GHz).

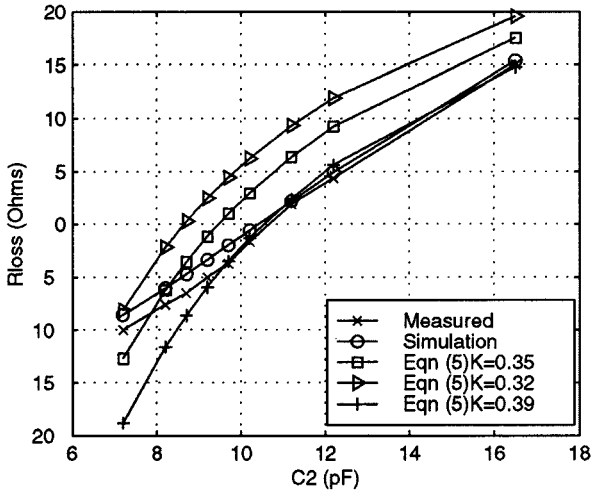

Fig. 5. Effective loss resistance tuning range as a function of C_2.

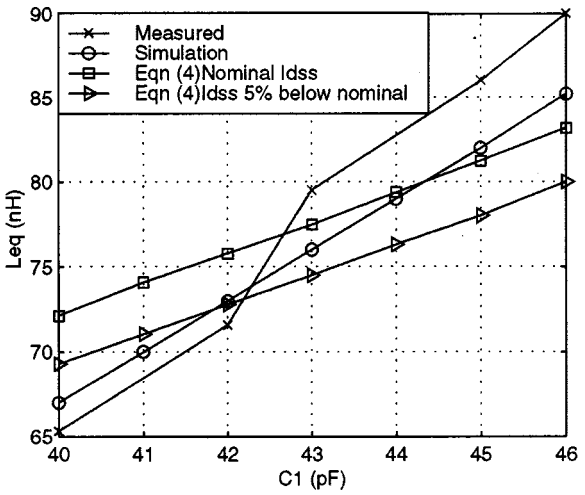

Fig. 7. Inductance tuning range as a function of C_1.

over a 25-Ω range of both positive and negative resistances corresponding to a 9.3-pF change in C_2. The measured and simulated series loss resistances are a near-linear function of the tuning capacitor C_2. Below 9 pF, the assumption that C_2 is much larger than the sum of parasitic capacitances is no longer valid, and R_{loss} predicted by (5) begins to diverge from measured and simulation results, as shown in Fig. 5. As shown, the effect of K in (5) is to shift the entire R_{loss} curve vertically while preserving the effective tuning range as C_2 is varied.

Tuning of the inductance is accomplished by varying C_1. As C_1 was varied, the ratio C_1/C_2 was held constant to ensure that R_{loss} stayed constant. Different inductance values were measured and plotted to give the set of curves shown in Fig. 6. The corresponding simulation results are also shown in Fig. 6 for the same tuning conditions. The excellent agreement between the simulations and measurements was obtained by adjusting the dc gate bias slightly to account for a wide variation in the saturated drain current of the FET's between test chips.

The self-resonant frequency of each inductance value measured was not affected by tuning of C_2. The measured inductance tuning range is shown in Fig. 7 along with expected values from simulation and (4). As in the case of loss resistance tuning, the inductance dependence on C_1 is also approximately a linear function.

Fig. 7 also shows the expected L_{eq} when I_{dss} is 5% below the nominal value for the process. As shown, the dynamic tuning

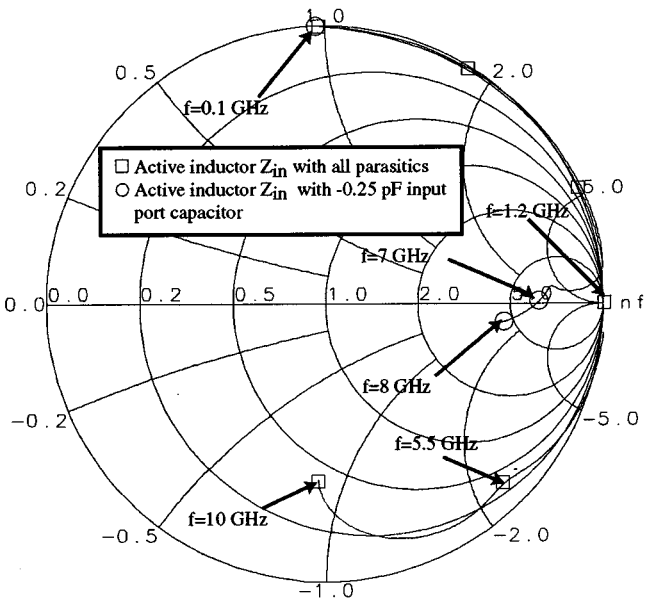

Fig. 8. Simulated effect of bandwidth limiting parasitic capacitors.

range of $L_{\rm eq}$ is not altered by variations in $I_{\rm dss}$. The wider dynamic range measured can be reflected in the simulations by changing the dc-bias conditions in the simulations. The smaller tuning range given by (4) is a result of neglecting the large channel conductance of the FET's. As shown in Figs. 5 and 7, (4) and (5) are reasonably accurate given their simplicity, and proven useful throughout the design of the circuit.

For a fixed inductance of 75 nH and no series loss, the input power level was swept from -30 to -0.9 dBm with negligible change in either the real or reactive component of $Z_{\rm in}$. Above -0.9 dBm, both $L_{\rm eq}$ and $R_{\rm loss}$ become strong functions of the input power, resulting from a change in the bias points of M_4 and M_8.

Simulation results show that electronic tuning can be easily introduced without compromising tuning range by replacing both C_1 and C_2 with varactor diodes. Since neither capacitor is grounded, each varactor diode must be placed in series with a fixed capacitance for dc blocking.

IV. Bandwidth Limiting Parameters

Analysis, simulation, and measurement results have shown that the active inductor equivalent circuit is an inductor in parallel with a fixed lossy capacitance for frequencies approaching 10 GHz. Simulation results shown in Fig. 8 confirm that it is this small capacitance that limits the self-resonant frequency of the active inductor to 1.1 GHz. Simulations also show that the circuit behaves as an ideal inductor at higher frequencies when this capacitance is removed or significantly reduced. This is also shown in Fig. 8, with an ideal -0.25-pF capacitor connected from the input to ground. With this shunt negative capacitance, the self-resonant frequency of the active inductor is increased from 1.2 to over 5 GHz.

Analysis and simulation results confirm that it is the capacitive parasitics of FET's M_3 and M_8 that collectively appear as an equivalent capacitance $C_{\rm eq}$ to ground, as shown in Fig. 9.

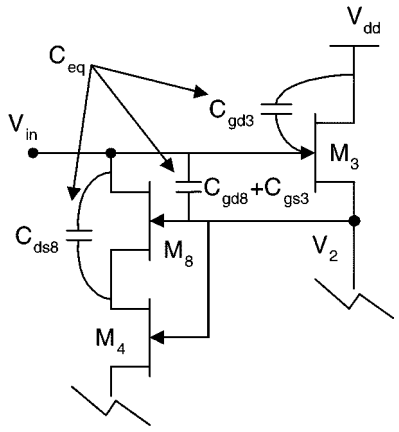

Fig. 9. Bandwidth limiting FET parasitic capacitors.

$C_{\rm ds8}$, $C_{\rm gd3}$, and $C_{\rm gd8}$ shown in Fig. 9, are negligible in comparison to $C_{\rm gs3}$ and, thus, $C_{\rm gs3}$ dominates the high-frequency performance of the circuit.

The effect of $C_{\rm eq}$ can be reduced in several ways to considerably extend the effective bandwidth of the inductor. Since a channel length of 1 μm was used for all FET's, the gatewidth required for a reasonable transconductance was also large, resulting in gate-to-source capacitances of the order of 0.6 pF. Simulation results show that a submicrometer process with a gate length less than 0.5 μm increases the inductor's effective bandwidth as a result of significantly lower gate-to-source capacitances.

Alternatively, use of a simple negative impedance converter (NIC) at the input port is being examined. A tunable negative capacitance with sufficiently low conductive loss could provide useful independent tuning of the parallel capacitance or remove it completely if desired. If the inductor is used in applications requiring an *LC* resonator, $C_{\rm eq}$ is desirable and can be left alone without any consequence to circuit performance.

V. Sensitivity to Parasitics

Detailed simulations have shown that the sensitivity of $Z_{\rm in}$ to parasitic contact lead resistance, inductance, and capacitance is negligible. The sensitivity of the realized inductance $L_{\rm eq}$ to finite drain conductance and parasitic FET capacitances is also very small, resulting in realized inductances that are accurately predicted by (4).

The loss resistance is insensitive to individual FET parasitics, but collectively these parasitics result in a measured $R_{\rm loss}$ that is not accurately predicted by (5), unless the parameter K is included. A fixed value of K between 0.3 and 0.4 results in (5), accurately predicting $R_{\rm loss}$ over the entire tuning range.

VI. Conclusion

An active inductor circuit has been developed with tunable inductance and independently tunable series loss resistance. Measurement results confirm the tuning control of both the inductance and loss resistance and the independence of the inductance from loss resistance tuning. Simple analytical expressions have been presented for both the inductance and series loss resistance. Analytic predictions and simulations were found to be

in good agreement with measured results. Electronic tuning of both the inductance and loss resistance can be achieved with varactor diodes.

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