A Fully Integrated Active Inductor with Independent Voltage Tunable Inductance and Series-Loss Resistance

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***Abstract*—A fully integrated GaAs MESFET active inductor is presented in this paper with independent voltage tunable inductance and series-loss resistance. The measured inductance is tunable from 65 to 110 nH in the frequency range from 100 MHz to 1.0 GHz. The measured loss resistance is independently tunable over a −5.6- to +20.8-Ω range corresponding to a 0.26 and 0.65 V change in dc tuning voltages, respectively.**

***Index Terms*—Active filters, inductors, MESFET integrated circuits, Q factor.**

I. Background

INTEGRATED inductors find application in many facets of radio-frequency integrated circuit (RFIC) design including impedance matching, filtering, biasing, and in oscillator circuits. For some of these applications, the added noise and linearity degradation introduced by active resonant circuits is acceptable. The advantage of using active circuits in place of passive designs is improved performance in terms of tuning functionality.

Realizing tunable resonators in integrated RF systems presents significant restraints in both size and tuning flexibility. As a result, off-chip structures are often used with considerably larger space requirements and package parasitics. If a resonator is to be implemented on-chip, passive *LC* networks are typically used. Since integrated spiral inductors have low-Q factors that can range from 10 to 30, these circuits are unsuitable for some applications.

Although high-quality capacitors can be reasonably integrated, inductors with sufficiently high-Q factors are difficult to integrate. In addition to this, space limitations limit passive inductors to values below 40 nH, above which the area consumed is no longer practical.

Active resonant circuits have allowed the small inductance limitation to be overcome. However, these circuits are often not tunable. Tunability in either the reactance or series-loss resistance is commonly achieved by replacing one or more capacitors with varactor diodes. This introduces many unwanted parasitics, as well as added space requirements to get a reasonable tuning range.

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With a suitable design, dc voltage tunability can be introduced without the use of varactor diodes. This offers greater tuning flexibility than a varactor diode provided the parameter to be tuned can be made sufficiently sensitive to the controlling voltage. One common means of accomplishing this is by varying the bias conditions for one or several devices in the circuit such that large changes in the device transconductance or channel conductance can be achieved.

This method was used by Lucyszyn and Robertson [1] in a novel circuit with both inductance and series-loss tunability. Their circuit realized an inductance that could be tuned over a small range of values, while the Q factor could also be set to be large at an arbitrary frequency. This circuit showed very narrow-band performance as a result of a strong frequency dependence of the series resistance realized by the circuit.

Alinikula *et al.* [2] described a different topology, which offered more flexible dc voltage tuning control. With this technique, an FET was biased in its linear region as a variable resistor allowing control of the frequency at which the lowest loss occurred. For narrow bandwidths, a large Q factor was realized, but as with the previous design, the loss resistance showed a strong frequency dependence.

A similar technique was used by Sinsky *et al.* [3] to introduce voltage tunability in several active impedance synthesizing circuits using second-generation current conveyors (CCII−). Tunability was accomplished by replacing a single resistor in a CCII− feedback network with a single FET with zero drain-to-source voltage bias. Each CCII− was implemented as a cascaded array of GaAs MESFETs to obtain sufficiently high gain. This required many large FETs in addition to off-chip biasing circuitry, resulting in significant space requirements on-chip.

DC tuning of the series-loss resistance was also used in a novel design described by Haigh [4]. An inductive circuit was implemented by using two integrators terminated in a capacitance and connected in a feedback loop realizing a gyrator action. Although the resonant frequency remained independent of series-loss resistance tuning, the circuit showed a large positive loss resistance for frequencies below the resonant frequency.

An alternative method of dc voltage tuning was proposed by Yong-Ho *et al.* [5], in which the positive supply voltage was used to tune the Q factor. The design expanded on a common Q enhancement method using a single FET with active inductive feedback. Although the inductance was tunable over a wide range by varying the loss resistance of the active feedback cir-

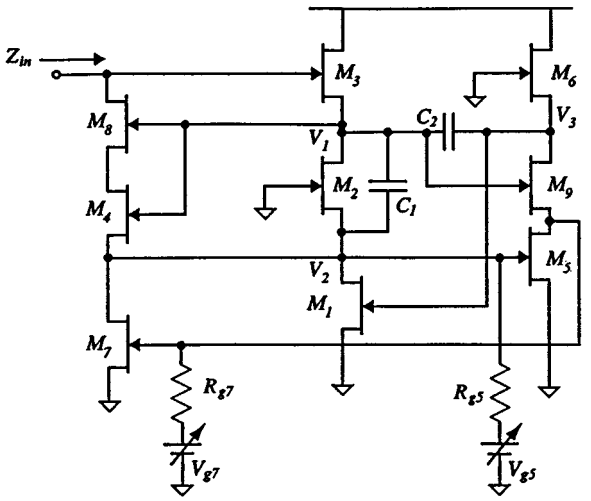

Fig. 1. Active inductor schematic without all dc-bias components.

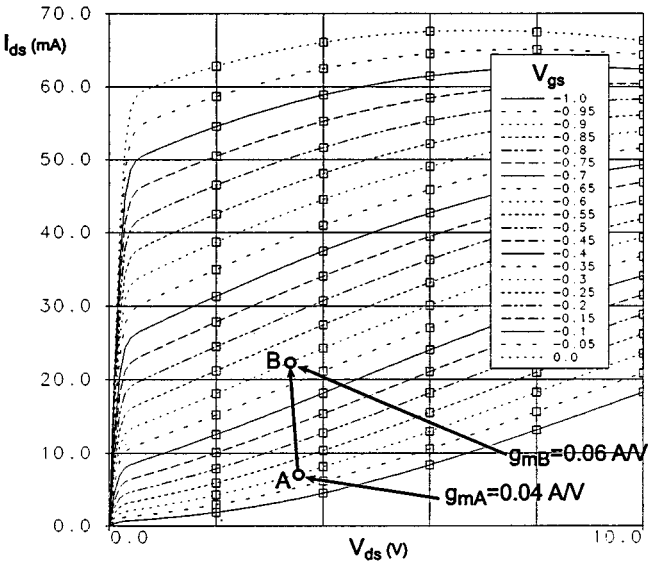

Fig. 2. FET dc operating points enabling voltage tuning of the transconductance.

cuit, the series loss could only be set to zero for a narrow range of frequencies.

In this paper, a novel active inductor topology presented in [6] has been adapted to offer dc voltage tuning control. In this design, an inductor with a series loss is realized where the series-loss resistance of the circuit remains frequency independent and tunable over a broad range of values including zero by changing the dc gate bias voltage of a single FET. The inductance is also independently voltage tunable over a wide range by changing the dc gate bias voltage of a second FET. With this new tuning method, tuning of either the inductance or the series loss has negligible impact on the other parameter and complete independence is maintained.

This is a significant improvement over the tuning method presented in [6], in which two separate capacitors were used to vary the inductance and series loss. With the capacitive tuning method previously proposed, the inductance remained independent of series-loss resistance tuning as the loss tuning capacitor was changed. Each inductance adjustment, however, required a single adjustment of the series-loss tuning capacitor to restore the loss back to the desired value. In addition to orthogonal tuning, this new tuning method introduces fewer parasitics than using varactor diodes and extends the inductance tuning range by an additional 20 nH in comparison to the capacitive tuning method.

II. Circuit Design

The schematic of the active inductor with dc tuning voltages is shown in Fig. 1. The circuit consists of two stages, including a voltage to current conversion at the input port and a six FET frequency-dependent voltage generator. The six FET voltage generator formed by M_1 to M_3, M_5, M_6, and M_9 generates two voltages V_1 and V_2 such that the difference $V_2 - V_1$ is a linear function of the input port voltage $v_{\rm in}$ and is proportional to the load impedance $1/sC_1$. By setting the input port current $i_{\rm in}$ proportional to $V_2 - V_1$ with a simple voltage-to-current conversion formed by M_4, M_7, and M_8, a gyrator action is achieved. This results in an input impedance that consists of an inductance $L_{\rm eq}$ and a series-loss resistance $R_{\rm eq}$.

Small-signal analysis of the circuit in Fig. 1 under the constraint that $g_{m5} = g_{m6} = g_{m9}$ results in expressions for $L_{\rm eq}$ and $R_{\rm eq}$ given as

$$L_{\rm eq} = \frac{A \cdot D \cdot \omega^2 + B \cdot C}{C^2 + D^2 \cdot \omega^2} \tag{1}$$

$$R_{\rm eq} = \frac{B \cdot D - A \cdot C}{D^2} \tag{2}$$

where

$$A = (2g_{m5} + g_{m1} + g_{m3})\, C_1 C_2$$

$$B = (g_{m2}g_{m3} + g_{m2}g_{m1} + g_{m4}g_{m5} - g_{m1}g_{m5})\, C_2 + g_{m5}\,(g_{m3} - g_{m1})\, C_1$$

$$C = g_{m3}g_{m4}g_{m5}\,(g_{m7} - g_{m1})$$

$$D = g_{m3}g_{m4}\,(g_{m1} + g_{m2})\, C_2.$$

The equivalent series inductance $L_{\rm eq}$ and series-loss resistance $R_{\rm eq}$ can be varied by changing the gate-bias voltages V_{g7} and V_{g5}, respectively. To enable independent voltage tuning of $R_{\rm eq}$ and $L_{\rm eq}$, M_7 and M_5 must be biased such that the transconductance g_m of each device is a strong function of its respective gate bias voltage. The bias points used for M_5 and M_7 in the described design are shown in Fig. 2.

With each device initially biased at 35% (Point B) of the steady-state maximum drain current $I_{\rm dss}$ (68 mA, in this case) as shown, a 0.04- to 0.06-A/V transconductance swing was achieved corresponding to a -0.9- to -0.6-V change in gate bias voltage. This allows V_{g7} to be used for tuning of $L_{\rm eq}$ by changing g_{m7}. Similarly, V_{g5} can be used for tuning of $R_{\rm eq}$ independently by changing g_{m5} over the same range.

The constraint on g_{m5}, g_{m6}, and g_{m9} is always maintained when g_{m5} is varied since M_5, M_6, and M_9 are in cascode and

have the same drain currents $I_{\rm ds}$ and, hence, the same transconductance provided each of the drain to source voltages are approximately equal. When $g_{m7} = g_{m2} = g_{m1} = g_{m4}$, $C = 0$ in (1) and (2) and $L_{\rm eq}$ and $R_{\rm eq}$ become

$$L_{\rm eq}|_{C=0} = C_1 \frac{g_{m2} + g_{m3} + 2g_{m5}}{2g_{m2}g_{m3}g_{m4}} \tag{3}$$

$$R_{\rm eq}|_{C=0} = \frac{g_{m2}^2 + g_{m2}g_{m3}}{2g_{m2}g_{m3}g_{m4}} + \frac{C_1}{C_2}\, g_{m5} \left(\frac{g_{m3} - g_{m2}}{2g_{m2}g_{m3}g_{m4}} \right) \tag{4}$$

which are the same equations given in [6], where capacitive tuning via C_1 and C_2 was used to adjust $L_{\rm eq}$ and $R_{\rm eq}$. Changing g_{m7} via V_{g7} enables dc voltage tunability of the inductance by introducing a mismatch between g_{m7} and g_{m1} making the C term in (1) and (2) nonzero. To get expressions for $L_{\rm eq}$ and $R_{\rm eq}$ as functions of their respective tuning voltage, an equation relating the FET transconductance to its corresponding bias conditions must be obtained. All theoretical results given by (1) and (2) in the following section are expressed in terms of transconductances to avoid complicated modeling and measurement of each device's transconductance as a function of its gate bias voltage. Many bias-dependent transconductance expressions exist in the literature [7] and can be adapted to model a specific process if theoretical voltage-dependent equations are required.

Independent tuning of $L_{\rm eq}$ and $R_{\rm eq}$ can only be achieved provided g_{m4}, g_{m2}, and g_{m3} change in proportion to g_{m7} as g_{m7} is varied. This is achieved by the circuit since g_{m7} is varied by changing its drain current I_{ds7}, which, in turn, causes a proportional change in the drain currents of M_4, M_2, and M_3 and, hence, their transconductances also change proportionally.

Since the drain of M_7 is connected to the drain of M_1, $I_{\rm ds2}$ and $I_{\rm ds4}$ will change proportionally to $I_{\rm ds7}$ when g_{m7} is varied, however, these currents will not be identical. For the results shown in the following section, the assumption $g_{m7} = g_{m2} = g_{m4}$ was made, which was confirmed by measurement and simulation to be a reasonable approximation.

For independent tuning of $L_{\rm eq}$ and $R_{\rm eq}$, $L_{\rm eq}$ must be independent of changes in g_{m5} and, similarly, $R_{\rm eq}$ must not be affected when g_{m7} is varied. When the approximation $g_{m7} = g_{m2} = g_{m4}$ is used, the predicted $L_{\rm eq}$ and $R_{\rm eq}$ given by (1) and (2) suggest a stronger interaction between $L_{\rm eq}$ and $R_{\rm eq}$ tuning than actually measured. Regardless of this, (1) and (2) do accurately predict the absolute values, as well as the actual measured tuning range of both $L_{\rm eq}$ and $R_{\rm eq}$.

The transconductance g_{m3} must be made much smaller than all other device transconductances and can be reasonably approximated in (1) and (2) as a linear function of g_{m7}. $R_{\rm eq}$ given by (2) is frequency independent and $L_{\rm eq}$ in (1) can also be approximated as frequency independent for frequencies higher than 100 MHz.

III. Results

The fabricated circuits used for all measurement results reported were implemented with a commercial 1-μm GaAs MESFET process. Since dc tunability of both the inductance and series-loss resistance is achieved by varying the dc-bias current of specific devices in the circuit, the total supply current varied over a 15–40-mA range using a 6-V supply. The die photo of the implemented circuit is shown in Fig. 3. The total chip area consumed was 900 μm $\times$ 700 μm.

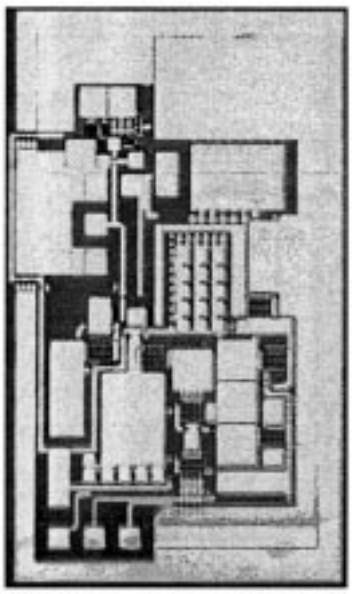

Fig. 3. Die photo of test circuit.

Simulation results using HP/EEsof Libra along with the measured effect of varying V_{g7} to tune the series equivalent inductance $L_{\rm eq}$ are shown in Fig. 4. As V_{g7} is made more negative, the drain current in M_7 decreases, while the drain current in M_1 remains unchanged because its gate bias voltage stays constant. This causes g_{m7}, g_{m2}, g_{m4}, and g_{m3} to decrease, resulting in an increase in the inductance in accordance with (1).

The theoretical effective tuning range of $L_{\rm eq}$ from (1) is shown in Fig. 5. The g_{m7} values used (0.04–0.06 A/V) correspond to the same tuning range in V_{g7} used in the measurements (from -0.59 to -0.85 V), resulting in a theoretical tuning range for $L_{\rm eq}$ from 55 to 102 nH, as compared to the 65–110-nH tuning range measured as shown in Fig. 4.

For very large inductance values, $R_{\rm eq}$ starts to increase as g_{m7} is made very small and M_7 is approaching cutoff. This is shown in Fig. 4 for the case when $V_{g7} = -0.85$ V resulting in an inductance of 110 nH. This effect is modeled by (2) as g_{m7} is made much smaller than g_{m1}.

Tuning of $R_{\rm eq}$ is accomplished by varying the gate bias voltage V_{g5}. As V_{g5} is made more negative, the drain currents in M_5, M_6, and M_9 decrease, resulting in a decrease in the transconductance of each device and, hence, a decrease in $R_{\rm eq}$. The simulated tuning range in $R_{\rm eq}$ is shown in Fig. 6. The corresponding measured series-loss curves are shown in Fig. 7 for the same tuning conditions and several other tuning values to demonstrate the wide dynamic tuning range in $R_{\rm eq}$. Fig. 8 shows the theoretical loss tuning range given by (2) as g_{m5}, g_{m6}, and g_{m9} are varied by changing V_{g5}. As shown in both Figs. 6 and 7, the inductance has little sensitivity to tuning of $R_{\rm eq}$.

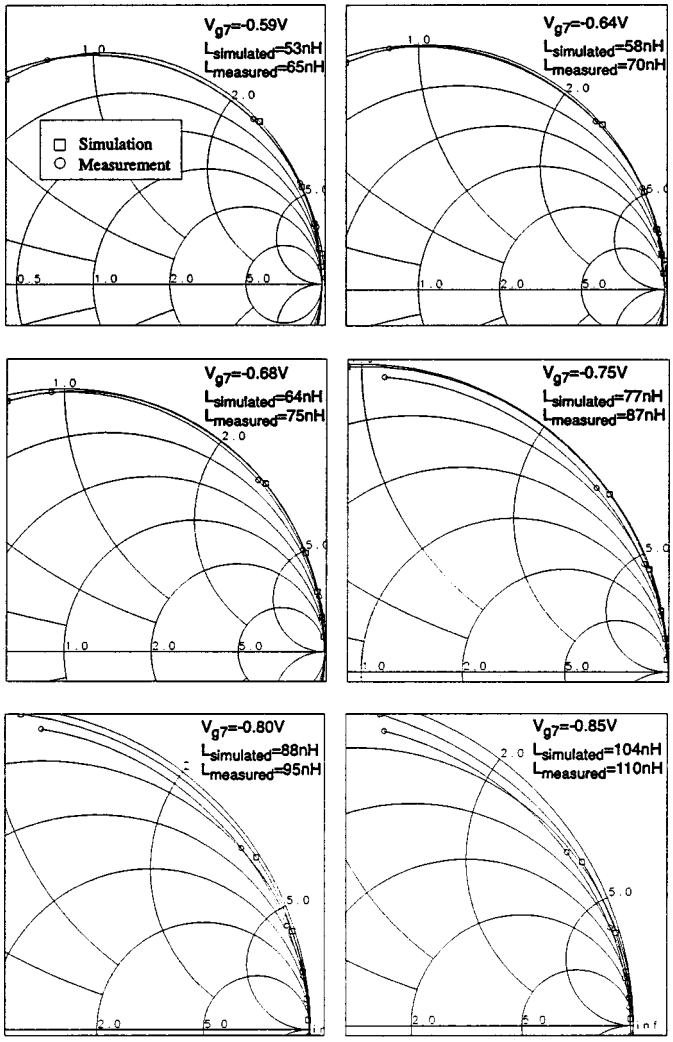

Fig. 4. Simulated and measured effect of varying the $L_{\rm eq}$ tuning voltage V_{g7} (0.1 GHz $< f <$ 1 GHz).

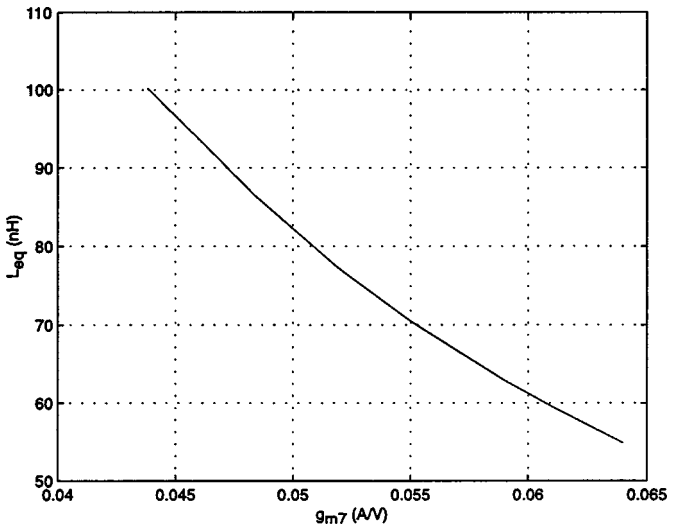

Fig. 5. Theoretical $L_{\rm eq}$ tuning range as g_{m7} is varied via V_{g7}.

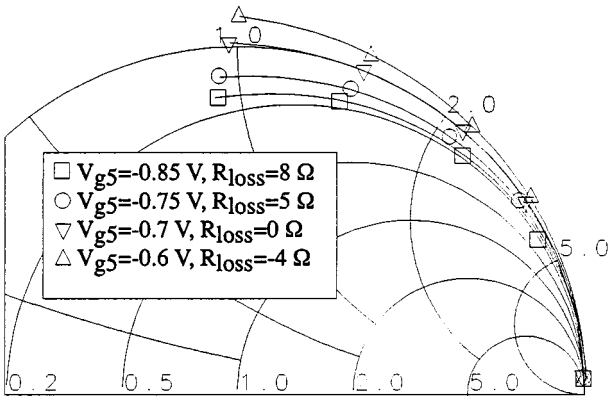

Fig. 6. Simulated effect of varying the loss resistance tuning voltage V_{g5} (0.1 GHz $< f <$ 1 GHz).

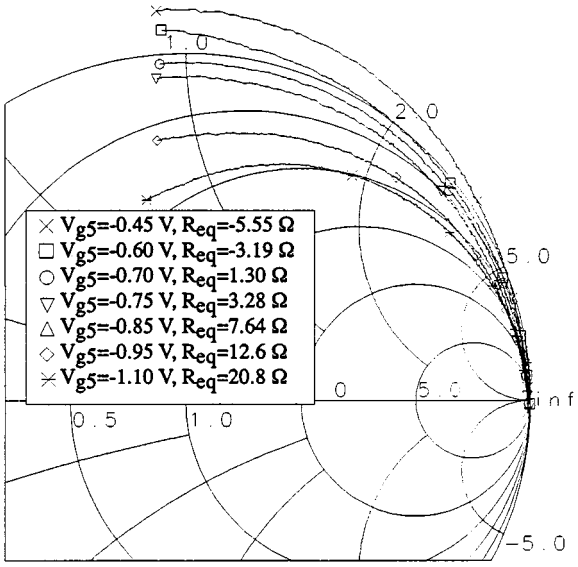

Fig. 7. Measured effect of varying the loss resistance tuning voltage V_{g5} (0.1 GHz $< f <$ 1 GHz).

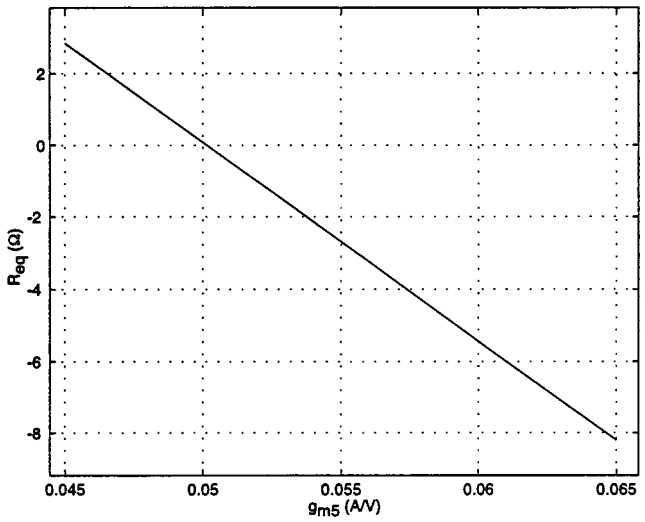

Fig. 8. Theoretical loss resistance tuning range as g_{m5} is varied via V_{g5}.

Simple first-order analysis shows that as g_{m7} is varied, a small series capacitance $C_{\rm eq}$ is added to the inductor equivalent circuit. The effects of this finite capacitance are a result of the mismatch introduced between g_{m7} and g_{m8}. This effect is

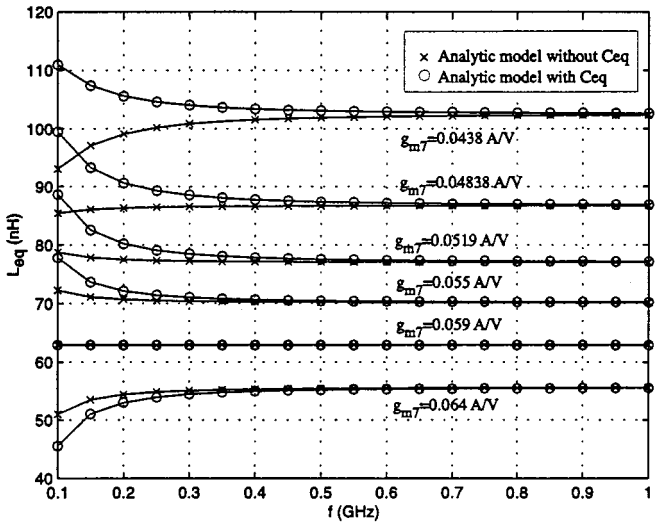

Fig. 9. Effects of finite series capacitance resulting from g_{m7} tuning.

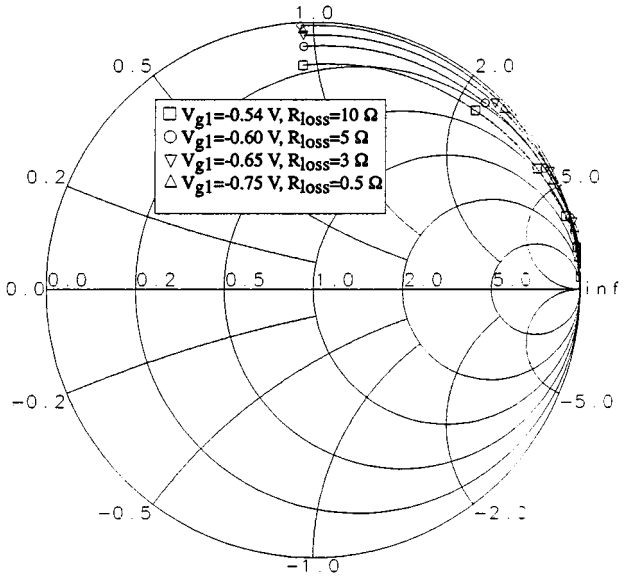

Fig. 10. Measured effect of varying V_{g1} to adjust the loss resistance (0.1 GHz $< f <$ 1 GHz).

shown in Fig. 9 over the effective bandwidth of the circuit. These effects are not apparent until low frequencies around 100 MHz. Analysis and measurements confirm that this capacitance always remains small and negligible regardless of g_{m5} provided that any change in g_{m5} is reflected in an equal change in both g_{m9} and g_{m6}.

For the results given, g_{m1} was set constant at 0.06 A/V. As shown in Fig. 9, $C_{\rm eq}$ has the greatest influence when $g_{m7} \approx 0.04$ A/V as a result of the larger mismatch between g_{m7} and g_{m1}. As this mismatch is decreased, the effects of $C_{\rm eq}$ become more negligible.

Use of V_{g5} to adjust the series-loss gives fully orthogonal tuning with respect to the inductance tuning via V_{g7}. Alternatively, it can be shown through a first-order analysis similar to that given previously that the gate bias voltage for FET M_1 shown in Fig. 1 can also be used to give reasonably independent tuning of $R_{\rm eq}$ over a limited range. The measured effect of varying this bias voltage V_{g1} is shown in Fig. 10. The measurement results show the introduction of a small reactive component when V_{g1} is used to tune $R_{\rm eq}$. This makes V_{g5} preferable for tuning $R_{\rm eq}$ since only the series real resistance is altered as V_{g5} is varied.

IV. Conclusion

A GaAs active inductor design has been presented with independently voltage adjustable inductance and series-loss resistance. Analytic expressions for the inductance and series-loss resistance have been presented. The circuit described was fabricated and tested in a commercial 1-μm GaAs MESFET process. First-order analysis, simulations, and measurements were found to be in good agreement.

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